Notice of Allowability	Application No.	Applicant(s)	
	09/888,025	DAVIES, BARRY STANLEY	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-3*.

3. ☒ The drawings filed on *25 June 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6-25-01
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *5/25/04* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. Lamarre
Primary Examiner

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven Santema #40156 on May 25, 2004.

The application has been amended as follows:

Claim 1 lines 4-5 originally read "...circuit having a one or more..."

Claim 1 lines 4-5 now reads "...circuit having one or more..."

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

The present invention relates to fault insertion in an integrated circuit. The present invention provides a system to induce faults in highly integrated circuits and provides a system that is independent of the boundary scan technique and resides in a functional portion of the integrated circuit. The system does not require faults be induced through manually grounding or forcing high accessible circuit nodes. The fault insertion system is microprocessor controlled through a Fault Control Register (FCR). The FCR comprises two registers: a Fault Identification Register (FIR), and a Fault Apply Register (FAR). The FIR is connected to a FIR decode block which, depending on the values contained in the FIR, applies signals to one or more node fault logic blocks connected to

nodes of the integrated circuit. The node fault logic blocks either apply a test signal to a circuit node, or apply the normal system signals to the node. The FAR controls an enable signal to the FIR decode block, and determines when, and the duration, that the test signal will be applied. An External Control Bit of the FAR also allows manual control of the test signal. The sole independent claim of the present invention presents a specific recitation of the circuit and specific functions such as "...a Fault Apply Register (FAR) operated to receive FAR codes from said source for register values, said FAR codes having values associated with a fault-on code and a fault-off code; a FAR decode block connected to said FAR and operated to decode said FAR codes and assert a FAR decode block output signal when said FAR contains said fault-on code, and to deassert said FAR decode block output signal when said FAR contains said fault-off code; an External Control Bit (EXT) operated to receive EXT values from said source for register values, said EXT values associated with set or not set; a first logic connected to said EXT and said external assert signal, and operated to assert a first logic output signal when said EXT contains said not set value or when said EXT contains said set value and said external assert signal is asserted; a second logic connected to said FAR decode block output signal and said first logic output signal, and operated to assert a second logic output signal when said FAR decode block output signal is asserted and said first logic output signal is asserted; a Fault Identification Register (FIR) operated to receive a FIR code from said source for register values, said FIR code being one of a set of FIR codes, each of said FIR codes having a value associated with a desired fault; a FIR decode block connected to said FIR and said second logic output signal, and

operated to decode said FIR code and assert a FIR decode block output signal while said second logic output signal is asserted; and a circuit node fault logic block connected to said FIR decode block output signal and one of said circuit nodes, and operated to apply said normal system signals to said circuit node when said FIR decode block output signal is not asserted, and to apply a test signal to said circuit node while said FIR decode block output signal is asserted."

The prior arts of record (Preston, U.S. Patent No. 5,938,779 as an example) teach an application specific integrated circuit (ASIC) including a standard boundary scan (BSCAN) interface, with a collateral test interface connected to the BSCAN interface by a signal line for exchanging information and connected to a memory device for storing or retrieving information. The memory device has a fault insertion register connected to the collateral test interface by a fault insertion information signal line. Or, it may include another type of memory device instead, such as a status memory or a provisioning memory connected to the collateral test interface via control logic (or, a selected combination of different memory devices). This circuit contains a provisioning/status interface with control logic for storing provisioning data and/or for retrieving stored status data. The fault insertion register can be connected to the BSCAN interface for storing fault insertion data. The prior arts however fail to teach the claimed specifics of the Fault Apply Register, FAR decode block, the external control bit and signal specific details as quoted above. As such, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the limitations set forth in the present application.

Moreover, none of the prior art of record, taken either alone or in combination, anticipates nor renders obvious the claimed inventions. Hence, claims 1-3 are allowable over the prior arts of record.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB
Cynthia Britt
Examiner
Art Unit 2133

Guy J. Lamarre
GUY J. LAMARRE
PRIMARY EXAMINER